REMARKS

Claims 1-10 remain in connection with the present application.

Elections of Species

The Examiner has alleged that the application contains claims directed to two (2) allegedly patentably distinct species as follows: a first embodiment depicted in at least Fig. 1; and a second embodiment depicted in at least Fig. 5. Accordingly, the Examiner has requested Applicant to elect a single species for prosecution on the merits in connection with the present application.

In reply to the Examiner's Election of Species, Applicant elects a first embodiment including at least Fig. 1 of the present application (presumably including Figs. 1-4 of the present application). This election is made without traverse.

At the present time, Applicant believes that at least claims 1-4 are readable upon the elected species. However, if the Examiner finds any of the claims of the present application to be generic and to be allowable, the allowance of each of claims 1-10 in connection with the present application is earnestly solicited.

CONCLUSION

An earlier indication of the allowablility of each of claims 1-10 in connection with the present application is earnestly solicited.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact the undersigned at the telephone number listed below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for

any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNESS, DICKEY, & PIERCE, P.L.C.

By _____
Donald J. Daley, Reg. No. 34,313

DJD/bof

P.O. Box 8910
Reston, Virginia 20195
(703) 668-8000

CURRENT LIST OF PENDING CLAIMS

1. (Original) A parallel/serial conversion circuit, comprising:

a parallel/serial conversion section for converting first parallel data to first serial data and converting second parallel data to second serial data; and

a shift clock signal generation section for generating a shift clock signal,

wherein the parallel/serial conversion section converts the first parallel data to the first serial data by shifting the first parallel data in response to the shift clock signal,

the parallel/serial conversion section converts the second parallel data to the second serial data by shifting the second parallel data in response to the shift clock signal,

a combination of the first serial data and the second serial data indicates bit separation, a logic value '0', or a logic value '1', and

the shift clock signal generation section generates the shift clock signal by combining the first serial data and the second serial data.

2. (Original) A parallel/serial conversion circuit according to claim 1, wherein:

the parallel/serial conversion section comprises a first shift register, a second shift register, a first pulse generation circuit, and a second pulse generation circuit;

the first and second parallel data each contain a plurality of bits;

the first serial data and second serial data are inverse to each other in terms of the bit value;

the first shift register shifts the first parallel data stored therein on a bit-by-bit basis in response to the shift clock signal to convert the first parallel data to third serial data;

the second shift register shifts the second parallel data stored therein on a bit-by-bit basis in response to the shift clock signal to convert the second parallel data to fourth serial data;

the first pulse generation circuit receives the third serial data and converts the third serial data to the first serial data based on each bit contained in the third serial data; and

the second pulse generation circuit receives the fourth serial data and converts the fourth serial data

to the second serial data based on each bit contained in the fourth serial data.

3. (Original) A parallel/serial conversion circuit according to claim 1, wherein a signal indicating the first serial data contains a first end data signal indicating an end of the first serial data, and a signal indicating the second serial data contains a second end data signal indicating an end of the second serial data.

4. (Original) A parallel/serial conversion circuit according to claim 1, further comprising a delay circuit for determining a delay time of the shift clock signal.

5. (Original) A serial data generation circuit for generating serial data containing a plurality of bits, comprising:

a serial data generation section for combining first serial data and second serial data generated by a parallel/serial conversion circuit to generate the serial data,

wherein a serial data signal indicating the serial data includes a signal for separating one bit from another in the plurality of bits contained in the serial data, and

the parallel/serial conversion circuit comprises:

a parallel/serial conversion section for generating the first serial data by converting first parallel data to the first serial data and generating the second serial data by converting second parallel data to the second serial data; and

a shift clock signal generation section for generating a shift clock signal,

wherein the parallel/serial conversion section converts the first parallel data to the first serial data by shifting the first parallel data in response to the shift clock signal,

the parallel/serial conversion section converts the second parallel data to the second serial data by shifting the second parallel data in response to the shift clock signal,

a combination of the first serial data and the second serial data indicates bit separation, a logic value '0', or a logic value '1', and

the shift clock signal generation section generates the shift clock signal by combining the first serial data and the second serial data.

6. (Original) A synchronization signal generation circuit for generating a synchronization signal indicating an end of serial data, wherein the serial data is generated by combining first serial data and second serial data generated by a parallel/serial conversion circuit, the synchronization signal generation circuit comprising:

a synchronization signal generation section for generating the synchronization signal based on a combination of a first end data signal contained in a signal indicating the first serial data and a second end data signal contained in a signal indicating the second serial data,

wherein the first end data signal indicates an end of the first serial data and the second end data signal indicates an end of the second serial data, and

the parallel/serial conversion circuit comprises:

a parallel/serial conversion section for generating the first serial data by converting first parallel data to the first serial data and generating the second serial data by converting second parallel data to the second serial data; and

a shift clock signal generation section for generating a shift clock signal,

wherein the parallel/serial conversion section converts the first parallel data to the first serial data by shifting the first parallel data in response to the shift clock signal,

the parallel/serial conversion section converts the second parallel data to the second serial data by shifting the second parallel data in response to the shift clock signal,

a combination of the first serial data and the second serial data indicates bit separation, a logic value '0', or a logic value '1', and

the shift clock signal generation section generates the shift clock signal by combining the first serial data and the second serial data.

7. (Original) A clock signal generation circuit for generating a clock signal, wherein the clock signal separates one bit from another in a plurality of bits contained in serial data, and the serial data is generated by combining first serial data and second serial data generated by a parallel/serial conversion circuit, the clock signal generation circuit comprising:

a clock signal generation section for generating the clock signal based on a combination of a first pulse

signal contained in a signal indicating the first serial data and a second pulse signal contained in a signal indicating the second serial data,

wherein the first pulse signal and the second pulse signal separate one bit from another in a plurality of bits contained in the serial data, and

the parallel/serial conversion circuit comprises:

a parallel/serial conversion section for generating the first serial data by converting first parallel data to the first serial data and generating the second serial data by converting second parallel data to the second serial data; and

a shift clock signal generation section for generating a shift clock signal,

wherein the parallel/serial conversion section converts the first parallel data to the first serial data by shifting the first parallel data in response to the shift clock signal,

the parallel/serial conversion section converts the second parallel data to the second serial data by shifting the second parallel data in response to the shift clock signal,

a combination of the first serial data and the

second serial data indicates bit separation, a logic value '0', or a logic value '1', and

the shift clock signal generation section generates the shift clock signal by combining the first serial data and the second serial data.

8. (Original) A serial data transmission device, comprising:

a parallel/serial conversion circuit comprising:

a parallel/serial conversion section for converting first parallel data to first serial data and converting second parallel data to second serial data; and

a shift clock signal generation section for generating a shift clock signal,

wherein the parallel/serial conversion section converts the first parallel data to the first serial data by shifting the first parallel data in response to the shift clock signal,

the parallel/serial conversion section converts the second parallel data to the second serial data by shifting the second parallel data in response to the shift clock signal,

a combination of the first serial data and the second serial data indicates bit separation, a logic value

'0', or a logic value '1', and

the shift clock signal generation section generates the shift clock signal by combining the first serial data and the second serial data.

9. (Original) A serial data reception device, comprising:

a serial data generation circuit for generating serial data containing a plurality of bits;

a synchronization signal generation circuit for generating a synchronization signal indicating an end of the serial data; and

a clock signal generation circuit for generating a clock signal,

wherein the serial data generation circuit generates the serial data by combining the first serial data and the second serial data generated by a parallel/serial conversion circuit,

a serial data signal indicating the serial data includes a bit separation signal separating one bit from another in the plurality of bits contained in the serial data,

the synchronization signal generation circuit generates the synchronization signal based on a combination of the first end data signal contained in a

signal indicating the first serial data and a second end data signal contained in a signal indicating the second serial data,

the first end data signal indicates an end of the first serial data and the second end data signal indicates an end of the second serial data,

the clock signal generation circuit generates the clock signal based on a combination of a first pulse signal contained in the signal indicating the first serial data and a second pulse signal contained in the signal indicating the second serial data,

the clock signal separates one bit from another in the plurality of bits contained in the serial data,

the first pulse signal and the second pulse signal separate one bit from another in a plurality of bits contained in the serial data, and

the parallel/serial conversion circuit comprises:

a parallel/serial conversion section for generating the first serial data by converting first parallel data to the first serial data and generating the second serial data by converting second parallel data to the second serial data; and

a shift clock signal generation section for

generating a shift clock signal,

wherein the parallel/serial conversion section converts the first parallel data to the first serial data by shifting the first parallel data in response to the shift clock signal,

the parallel/serial conversion section converts the second parallel data to the second serial data by shifting the second parallel data in response to the shift clock signal,

a combination of the first serial data and the second serial data indicates bit separation, a logic value '0', or a logic value '1', and

the shift clock signal generation section generates the shift clock signal by combining the first serial data and the second serial data.

10. (Original) A serial data transmission system, comprising:

a serial data transmission device comprising a parallel/serial conversion circuit for generating first serial data and second serial data;

a serial data reception device for receiving the first serial data and the second serial data;

a first transmission path for transmitting the first serial data from the serial data transmission device

to the serial data reception device; and

a second transmission path for transmitting the second serial data from the serial data reception device to the serial data transmission device,

wherein the parallel/serial conversion circuit comprises:

a parallel/serial conversion section for generating the first serial data by converting first parallel data to the first serial data and generating the second serial data by converting second parallel data to the second serial data; and

a shift clock signal generation section for generating a shift clock signal,

wherein the parallel/serial conversion section converts the first parallel data to the first serial data by shifting the first parallel data in response to the shift clock signal, the parallel/serial conversion section converts the second parallel data to the second serial data by shifting the second parallel data in response to the shift clock signal, a combination of the first serial data and the second serial data indicates bit separation, a logic value '0', or a logic value '1', and the shift clock signal generation section generates the shift clock signal by combining the first serial data and the second

serial data,

the serial data reception device comprises a serial data generation circuit for generating serial data containing a plurality of bits, a synchronization signal generation circuit for generating a synchronization signal indicating an end of the serial data, and a clock signal generation circuit for generating a clock signal,

the serial data generation circuit generates the serial data by combining the first serial data and the second serial data,

a serial data signal indicating the serial data includes a bit separation signal separating one bit from another in the plurality of bits contained in the serial data,

the synchronization signal generation circuit generates the synchronization signal based on a combination of the first end data signal contained in a signal indicating a first serial data and a second end data signal contained in a signal indicating the second serial data,

the first end data signal indicates an end of the first serial data and the second end data signal indicates an end of the second serial data,

the clock signal generation circuit generates the

clock signal based on a combination of a first pulse signal contained in the signal indicating the first serial data and a second pulse signal contained in the signal indicating the second serial data,

the clock signal separates one bit from another in the plurality of bits contained in the serial data,

the first pulse signal separates and the second pulse signal separate one bit from another in a plurality of bits contained in the serial data.